EXHIBIT D

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571-272-7822

Paper 57
Date: May 11, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GOOGLE LLC,
Petitioner,

v.

SINGULAR COMPUTING LLC,
Patent Owner.

IPR2021-00179
Patent 8,407,273 B2

Before JUSTIN T. ARBES, STACEY G. WHITE, and JASON M. REPKO, *Administrative Patent Judges.*

PER CURIAM.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)
Dismissing Patent Owner's Motion to Exclude
37 C.F.R. § 42.64
Granting Patent Owner's and Petitioner's Motions to Seal
37 C.F.R. §§ 42.14, 42.54

B. Related Matters

The parties indicate that the '273 patent is the subject of *Singular Computing LLC v. Google LLC*, Case No. 1:19-cv-12551-FDS (D. Mass.) ("the district court case"). *See* Pet. xi; Paper 8, 1. Petitioner filed another petition challenging claims 1–70 of the '273 patent in IPR2021-00178, which was denied, and filed four other petitions challenging claims of two related patents also asserted in the district court case in IPR2021-00154 (denied), IPR2021-00155 (instituted), IPR2021-00164 (denied), and IPR2021-00165 (instituted).

C. The '273 Patent

The '273 patent, entitled "Processing with Compact Arithmetic Processing Element," issued on March 26, 2013. Ex. 1001, codes (45), (54). The '273 patent describes "computer processors or other devices which use low precision high dynamic range (LPHDR) processing elements to perform computations (such as arithmetic operations)." *Id.* at col. 5, l. 65–col. 6, l. 2. According to the '273 patent, conventional central processing unit (CPU) chips make inefficient use of transistors as a tradeoff for delivering the high precision required by many applications. *Id.* at col. 3, ll. 7–22. For example, conventional CPU chips "perform[] exact arithmetic with integers typically 32 or 64 bits long and perform[] rather accurate and widely standardized arithmetic with 32 and 64 bit floating point numbers," but require "on the order of a million transistors to implement the arithmetic operations." *Id.* at col. 3, ll. 15–22. According to the '273 patent, "many economically important applications . . . are not especially sensitive to precision and . . . would greatly benefit, in the form of application performance per transistor, from the ability to draw upon a far greater

fraction of the computing power inherent in those million transistors." *Id.* at col. 3, ll. 23–28. But "[c]urrent architectures for general purpose computing fail to deliver this power." *Id.* at col. 3, ll. 28–29.

The '273 patent is, therefore, "directed to a processor or other device, such as a programmable and/or massively parallel processor or other device, which includes processing elements designed to perform arithmetic operations . . . on numerical values of low precision but high dynamic range ('LPHDR arithmetic')." *Id.* at col. 2, ll. 11–18. According to the '273 patent, "'low precision' processing elements perform arithmetic operations which produce results that frequently differ from exact results by at least 0.1%." *Id.* at col. 2, ll. 28–31. In addition, "high dynamic range" processing elements "are capable of operating on inputs and/or producing outputs spanning a range at least as large as from one millionth to one million." *Id.* at col. 2, ll. 35–39.

Figure 6 of the '273 patent is reproduced below.

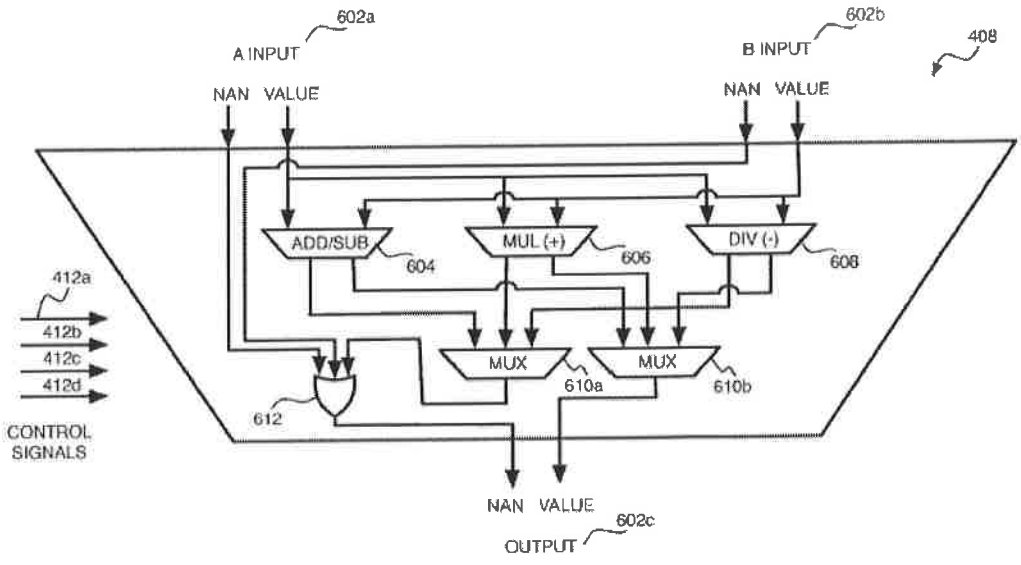

FIG. 6